third preferred embodiment are given the same reference numerals, and redundant descriptions thereof will be omitted.

Like the third preferred embodiment, the present preferred embodiment can also reduce the switching loss. In addition, unlike the third preferred embodiment, the fourth preferred embodiment has no limitations such as the need to dispose the p^+ region **15** and the trench-covering well region **16**B or the isolated well regions **16**F on the top surface S**1** without overlapping. This increases the degree of flexibility in the layout of each region. In FIG. **11**, for example, the arrangement pattern of the p^+ region **15** on the top surface S**1** corresponds to the vertices of rectangles, and there is found no specific relationship with the arrangement pattern of the isolated well regions **16**F.

Note that the interval of the isolated well regions **16**F in FIG. **11** is made smaller than that in FIG. **8**. Moreover, the isolated well regions **16**F are arranged in a hexagonal closest packed configuration on the top surface S**1** of the semiconductor substrate **73**. This reduces the cycle of change in impurity concentration on the top surface of the semiconductor substrate in the FWD region **82**, thus increasing the uniformity of the distribution of impurity concentrations in the top surface S**1**. It is thus possible to improve the recovery characteristics.

Fifth Preferred Embodiment

Referring to FIGS. **12** to **14**, a semiconductor substrate **75** of an RC-IGBT **95** according to the present preferred embodiment includes an n^+ cathode layer **7** (first layer), an n layer **50** (second layer), and a p layer **45** (third layer).

The p layer **45** is provided on the top surface S**1** and away from the back surface S**2**. The p layer **45** is at least partially included in the FWD region **82** and is in contact with the n layer **50**. The p layer **45** includes a p region **14** (first region) and a plurality of p^+ regions **15** (second regions). The p region **14** is provided on the entire top surface S**1** in the FWD region **82**. The p region **14** may be collectively formed together with the p base layer **2**. The p^+ regions **15** are spaced from one another on the p region **14**. When impurity concentrations in the direction parallel to the top surface S**1** of the semiconductor substrate **75** are compared, the p^+ regions **15** have a higher impurity concentration than that of the p region **14**.

The interlayer insulating film **10** is provided on the top surface S**1** of the semiconductor substrate **75** and has diode contact holes CF that expose part of the p layer **45**. The emitter electrode **11** is provided on the interlayer insulating film **10** and is in contact with the p layer **45** through the diode contact holes CF. The emitter electrode **11** is in contact with only the p^+ regions **15** of the p layer **45**.

The average impurity concentration of the p layer **45** is desirably reduced to a value close to the impurity concentration of the p region **14**. To achieve this, the ratio of the p^+ regions **15** occupying the p region **14** may be sufficiently reduced. The p^+ regions **15** are desirably arranged with small variations in distribution on the top surface S**1**, and for example, arranged in a hexagonal closest packed configuration as illustrated in FIG. **12**.

Note that constituent elements other than those described above are substantially the same as those of the above-described first preferred embodiment. Thus, constituent elements that are the same as or correspond to those of the first preferred embodiment are given the same reference numerals, and redundant descriptions thereof will be omitted.

According to the present preferred embodiment, the p region **14** having a lower impurity concentration than that of the p^+ regions **15** is formed on the entire top surface S**1** in the p layer **45** of the FWD region **82**. Consequently, the p layer **45** can be formed with a low impurity concentration and high uniformity in the FWD region **82**. This suppresses the recovery current in the FWD region **82**.

On the other hand, the emitter electrode **11** is in contact with only the p^+ regions **15** of the p layer **45**. This prevents the forward voltage in the FWD region **82** from increasing due to a voltage drop at a contact between the emitter electrode **11** and a portion of the p layer **45** that has a low impurity concentration.

From the above, the FWD region **82** can combine both a low forward voltage and a low recovery current. Using this FWD region **82** as a free-wheeling diode of the IGBT region **81** can reduce the switching loss of the RC-IGBT **95**.

In addition, when the IGBT region **81** includes a plurality of cells, it is possible for cells that have other cells adjacent thereto to avoid a situation where they are adjacent to the n^+ cathode layer **7** on the back surface S**2**. In other words, no anode-short structures are formed. Thus, snapback does not occur during forward bias operation in the FWD region **82**. It is thus possible to suppress an increase in steady-state loss due to snapback.

Sixth Preferred Embodiment

Referring to FIGS. **15** to **17**, a semiconductor substrate **76** of an RC-IGBT **96** according to the present preferred embodiment has trenches TR and a carrier storing layer **3** in not only the IGBT region **81** but also the FWD region **82**. The p layer **45** is disposed on the carrier storing layer **3**, and the trenches TR pass through both of these layers.

Note that constituent elements other than those described above are substantially the same as those of the above-described fifth preferred embodiment. Thus, constituent elements that are the same as or correspond to those of the fifth preferred embodiment are given the same reference numerals, and redundant descriptions thereof will be omitted.

According to the present preferred embodiment, the carrier storing layer **3** disposed under the p layer **45** can suppress the implantation of carriers from the p layer **45**. This further suppresses the recovery current. In addition, the trenches TR formed in the FWD region **82** allows a high withstand voltage to be kept in a state in which the carrier storing layer **3** is disposed in the FWD region **82**.

Seventh Preferred Embodiment

Referring to FIGS. **18** to **20**, in a semiconductor substrate **77** of an RC-IGBT **97** according to the present preferred embodiment, a p layer **47** includes a p region **14** (first region), a p^+ region **15** (second region) that is disposed away from the p region **14**, and a diffusion region **18** that connects the p region **14** and the p^+ region **15**. When impurity concentrations in the direction parallel to the top surface S**1** of the semiconductor substrate **77** are compared, the diffusion region **18** has a lower impurity concentration than those of the p region **14** and the p^+ region **15**. The emitter electrode **11** is in contact with only the p^+ region **15** of the p layer **47**.

Note that constituent elements other than those described above are substantially the same as those of the above-described fifth preferred embodiment. Thus, constituent elements that are the same as or correspond to those of the